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Docket No.: 02008/071003
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Masahiro Ishida et al.

Application No.: 10/779,904

Confirmation No.: 9608

Filed: February 17, 2004

Art Unit: 2436

For: METHOD AND APPARATUS FOR DEFECT
ANALYSIS OF SEMICONDUCTOR
INTEGRATED CIRCUIT

Examiner: O. A. Louie

REPLY UNDER 37 CFR §1.116

MS: AFTER FINAL
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Madam:

In response to the final Office Action dated January 15, 2009, please reconsider
this application in view of the following.